Attorney Docket No. 46872/269148
PATENT

Application No. 10/075,917 Filed: February 13, 2002

REMARKS

This Amendment and Response is being submitted in response to the Office Action mailed July 25, 2007. Applicant appreciates the time that Examiner took to interview the case with the inventor and with Applicant's representative on July 14, 2006.

Claims 1, 3-7, and 9-27 are pending in the application. Claim 1 stands provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of co-pending Application No. 10/803,690. Claims 1-21 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over U.S. 5,682,519 to Saldanha, *et al.* (hereinafter "Saldanha") in view of U.S. 4,792,909 to Serlet (hereinafter "Serlet"). Claims 22-27 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Saldanha in view of Serlet and further in view of U.S. 6,385,757 to Gupta (hereinafter "Gupta"). Applicant respectfully traverses the Examiner's rejections.

In the amendment above, Applicant has amended claims 1. No new matter is added by these amendments and support for these amendments may be found in the specification and claims as originally filed. Reconsideration of the claims is respectfully requested in view of the amendments above and remarks below.

I. Claims 1-21

Claims 1-21 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over U.S. 5,682,519 to Saldanha in view of Serlet. To establish a *prima* facie case of obviousness, the prior art references when combined must teach or suggest all of the claim limitations. Respectfully, neither Saldanha nor Serlet alone or when combined teaches or suggests all the claim limitations of claims 1 and 3-21. Claim 2 was previously cancelled, and the rejection of claim 2 is thus moot.

In claim 1, as amended, Applicant claims "[a] processor comprising: a Boolean logic unit formed in a static circuit with a static data path, wherein the Boolean logic unit is operable for dynamically performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations; and ... a plurality of registers, wherein the plurality of registers includes: a first register for storing the outcome of the most recently

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evaluated intra-conjunct term, and a second register for storing the outcome of the most recently evaluated conjunct." Neither Saldanha nor Serlet teach or suggest "[a] processor comprising: a Boolean logic unit formed in a static circuit with a static data path, wherein the Boolean logic unit is operable for dynamically performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations; and ... a plurality of registers, wherein the plurality of registers includes: a first register for storing the outcome of the most recently evaluated intra-conjunct term, and a second register for storing the outcome of the most recently evaluated conjunct."

Saldanha teaches building a circuit to physically represent a particular Boolean expression. Certain portions of the circuit are omitted to save power if they do not affect the result, i.e., the data path changes. Saldanha modifies the data path to use only the minimum number of components required to compute a predetermined operation or computation. See, e.g., Saldanha, Col. 6:6-42. The circuit is not "formed in a static circuit with a static data path" and is unable to "dynamically perform the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations" as Applicant has claimed in claim 1.

In Saldanha's circuit, the electrical signal must propagate through the entire circuit that represents the entire Boolean expression. The short-circuiting described in Saldanha is a means for optimizing a data path for an expression. The circuit still must evaluate all data input to the circuit. See, e.g., Saldhana, Col. 8:47-64. In contrast, Applicant claims a process for short-circuiting based on the data that is provided to the Boolean logic unit, i.e., the process eliminates evaluations when the inputs dictate that the overall result of the expression or conjunct can be short-circuited.

Serlet is introduced as teaching a "static Boolean circuit." *See* Office Action, page 4. Serlet does not cure the deficiencies of Saldanha. Thus, claim 1 is patentable over Saldanha in view of Serlet. Claims 3-7, 9-12, and 13-21 depend from claim 1 and are patentable for at least the same reasons. Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 3-7, 9-12, and 13-21.

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II. Claims 22-27

Claims 22-27 stand rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Saldanha in view of Serlet and further in view of Gupta. To establish a prima facie case of obviousness, the prior art references when combined must teach or suggest all of the claim limitations. As discussed above, neither Saldanha nor Serta alone or when combined teaches or suggests all the claim limitations of claim 1. Claims 22-27 depend from claim 1 and are allowable over Saldanha and Serta for at least the same reasons. Gupta does not cure the deficiencies of Saldanha in view of Serta.

Claims 22-27 depend from claim 1. In claim 1, as amended, Applicant claims "[a] processor comprising: a Boolean logic unit formed in a static circuit with a static data path, wherein the Boolean logic unit is operable for dynamically performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations; and ... a plurality of registers, wherein the plurality of registers includes: a first register for storing the outcome of the most recently evaluated intra-conjunct term, and a second register for storing the outcome of the most recently evaluated conjunct." None of Saldanha, Serta, and Gupta alone or when combined teaches or suggests "[a] processor comprising: a Boolean logic unit formed in a static circuit with a static data path, wherein the Boolean logic unit is operable for dynamically performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations; and ... a plurality of registers, wherein the plurality of registers includes: a first register for storing the outcome of the most recently evaluated intra-conjunct term, and a second register for storing the outcome of the most recently evaluated conjunct." Thus claim 1 is allowable over Saldanha in view of Serta and further in view of Gupta. Since claims 22-27 depend from claim 1, claims 22-27 are allowable as well. Applicant respectfully requests the Examiner withdraw the rejection of claims 22-27.

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III. Conclusion

Applicants respectfully submit that claims 1-27 are allowable. A favorable Office Action is respectfully solicited.

Should the Examiner have any comments, questions or suggestions of a nature necessary to expedite the prosecution of the application or to place the case in condition for allowance, the Examiner is courteously requested to telephone the undersigned at the number listed below.

Respectfully submitted,

Date: Oct. 25, 2007

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